IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	10/797,876
Applicants:	Dip et al.
Art Unit:	2811
Examiner:	Matthews, Colleen Ann
Title:	**SILICON GERMANIUM SURFACE LAYER FOR HIGH-K DIELECTRIC INTEGRATION**
Attorney Docket:	TPS-007
Confirmation No.:	5070

September 10, 2009

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
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Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicants request review of the rejections in the above-identified application set forth in the Final Office Action dated June 10, 2009. No amendments are being filed with this request, and it is being filed concurrently with a Notice of Appeal. Claims 1–8, 10, 11, 13–21, and 26–28 are pending of which claim 21 is withdrawn and claims 1–8, 10, 11, 13–20, and 26–28 stand rejected. Applicants request review of the rejections of all rejected claims, for the reasons set out hereinbelow.

REMARKS/ARGUMENTS FOR REVIEW

Claims 1–3, 13–16, 18–20, and 26–28 stand rejected under 35 U.S.C. §103(a) as being allegedly obvious over U.S. Patent No. 6,632,729 to Paton ("Paton") in view of Effects of low-temperature water vapor annealing of strained SiGe surface-channel pMOSFETs with high-k dielectric to Westlinder et al. ("Westlinder") and U.S. Patent No. 6,909,151 to Hareland et al. ("Hareland"). Claims 4–8, 10–11, and 17 are also rejected over the same combination of references, in further combination with EP 0684 650 B1 to Hiroshi et al. ("Hiroshi"), U.S. Pub. No. 2003/0218189 to Christiansen et al. ("Christiansen"), or U.S. Patent No. 5,259,881 to Edwards et al. ("Edwards"). Claims 1, 20, and 26 are independent claims. Claims 2–8, 10–11, and 17 depend directly or indirectly from claim 1, and claims 27 and 28 depend directly from claim 26. Applicants request review on the basis of Examiner's omission of an essential element required to establish a *prima facie* rejection. Obviousness is a question of law based on

underlying factual inquiries. The factual inquiries were enunciated by the Court in *Graham v. John Deere Co.*, 148 USPQ 459 (1966). The key to supporting any rejection under 35 U.S.C. §103 is the clear articulation of the reason(s) why the claimed invention would have been obvious in view of all of the factual information. See *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (2007). Applicants submit that Examiner consistently fails to provide a valid, objective analysis that could be considered a proper determination of obviousness under 35 U.S.C. §103(a).

Examiner correctly notes that Paton fails to disclose (i) forming a SiGe surface layer having an average Ge content of less than about 10 at.% on a Si substrate where the SiGe surface layer has an unreacted portion in contact with the substrate and (ii) oxidizing a surface portion of a SiGe surface layer wherein oxidizing the surface portion substantially prevents oxidation of the Si substrate during a depositing of a high-k dielectric layer or during an annealing process after depositing the high-k dielectric layer according to the claimed invention. (See OFFICE ACTION at page 4, ¶¶3–4, to the top of page 5.) Examiner references Westlinder and Hareland for this missing subject matter. Examiner alleges that it would have been obvious for one of ordinary skill in the art to modify Paton in view of Hareland to include a SiGe surface layer as taught by Westlinder in order to improve device properties such as channel mobility and stability. (See page 4, ¶3, and page 5, ¶1.)

Applicants submit that Examiner fails to state a valid, objective rationale for making the combination. (RESPONSE TO FINAL REJECTION dated August 10, 2009, at page 10, ¶¶2–3.) Specifically, Examiner's reason does not logically follow from the references themselves. Paton describes that a low-k silicon oxide layer formed on Si-containing substrates disadvantageously increases the Effective Oxide Thickness (EOT). That is, the low-k silicon oxide layer mitigates the benefit of the use of a high-k dielectric layer. (See Paton, col. 2, ll. 47–49.) Applicants submit that Paton, therefore, contradicts Examiner's reasoning and that one of ordinary skill in the art would not have a reasonable expectation of successfully making the proposed combination to improve device properties. Therefore, Examiner's reason fails to support the conclusion. Examiner has not established a *prima facie* case of obviousness.

In addition, Applicants submit that Westlinder fails to factually support Examiner's case. (RESPONSE TO FINAL REJECTION at the middle of page 11.) Examiner alleges that because Westlinder does <u>not</u> describe an oxide between the SiGe layer and the substrate, Westlinder discloses that oxidizing the surface portion of the SiGe surface layer substantially

prevents oxidation of the Si substrate according to the claimed invention. (See OFFICE ACTION at page 4, ¶4.) Examiner suggests that Fig. 1 of Westlinder supports this interpretation.

Applicants submit that Examiner ignores the facts. (See RESPONSE TO FINAL REJECTION at page 12, ¶3.) In Westlinder, Fig. 1 depicts a "schematic" picture of an ALD gate stack. (See Westlinder, page 525, 2nd sentence of "2. Experimental" paragraph.) Fig. 1 does not represent reality. Applicants specifically note that Westlinder describes an oxide layer on the SiGe layer, but Westlinder does not show the oxide layer in Fig. 1. In short, the absence of a layer between the Si buffer and the SiGe layer in Fig. 1 means nothing.

In addition to not depicting a layer between the Si buffer and the SiGe layer in Fig. 1, Westlinder does not describe the interface between the SiGe layer and the Si substrate–at all. Westlinder is silent regarding this interface because the interface between the SiGe layer and the Si buffer was not the focus of Westlinder's study. Rather, Westlinder focuses "on the interface between the high-k dielectric and the SiGe surface channel … ." (See page 525, top of right column.) Westlinder's silence cannot teach nor can it suggest anything to one of ordinary skill in the art.

Examiner also ignores the facts that Westlinder's "native" oxide layer is clearly formed before depositing the high-k layer, thus it is not formed between the layers, and that Westlinder's "native" oxide layer is formed via a wet chemical process. (See RESPONSE TO FINAL OFFICE ACTION at the bottom of page 11.) In other words, Westlinder's "native" oxide layer is formed at a different time and in a different manner than what is claimed. Therefore, it is not logical for Examiner to suggest that Westlinder's "native" oxide layer would necessarily prevent oxidation of the Si substrate in the same way as an oxide layer formed according to the claimed invention. Because Westlinder is silent regarding the interface between the Si buffer layer and the SiGe layer, and because Westlinder's oxide layer is formed at the different time via a different technique, Examiner cannot rely on Westlinder for describing that oxidizing the surface portion of the SiGe surface layer substantially prevents oxidation of the Si substrate, as claimed.

Applicants additionally submit that Examiner fails to reconcile why one of ordinary skill in the art would ignore the higher Ge content described in Westlinder (i.e., $Ge_{0.2}Si_{0.8}$ or 20 at.% Ge and $Ge_{0.3}Si_{0.7}$ or 30 at.% Ge) in favor of the Ge content of Hareland. (See RESPONSE TO FINAL REJECTION at page 13, ¶2.) Applicants submit that no objective reason exists and that Examiner is picking and choosing among the references using Applicants' claims

as a guide. For at least these reasons, Examiner has failed to establish a *prima facie* case of obviousness. Applicants request withdrawal of the rejections.

Because claims 2, 3, 13–16, 18, and 19 depend directly or indirectly from amended claim 1, Applicants submit that these claims are also patentable for at least the same reasons discussed above. (RESPONSE TO FINAL REJECTION at page 13, ¶2.)

In addition, regarding claim 20, Examiner notes that Paton fails to explicitly disclose the oxide layer formed by exposing the substrate to an oxygen containing gas. Examiner alleges that Westlinder discloses an oxide layer formed by exposing the substrate to a water vapor anneal. (OFFICE ACTION at page 8, ¶1.) Again, Applicants submit that these statements ignore the facts. (RESPONSE TO FINAL REJECTION at page 14.) As noted above, the oxide layer that Examiner references is formed prior to depositing the high-k dielectric layer via wet chemical oxidation. Therefore, it is not formed by exposing the wafer to an oxygen-containing gas. Furthermore, Westlinder states that, in conjunction with the discussion of Fig. 7 on page 527, and with regard to the $Al_2O_3/Si_{0.8}Ge_{0.2}$ stack, "no reaction has taken place among the materials in the gate stack." Applicants submit that oxidation is by definition a reaction. Westlinder's oxide layer is already present prior to water vapor annealing, and Westlinder explicitly states that no reaction occurs due to exposure to water vapor. Therefore, Examiner cannot rely on Westlinder for describing or suggesting oxidizing the surface portion of the SiGe surface layer by exposing the SiGe surface layer to an oxygen-containing gas, as claimed.

Regarding claims 4–8, Examiner references Hiroshi as disclosing forming the SiGe surface layer by exposing the substrate to a process gas including a Ge-containing gas comprising at least one of GeH_4 or $GeCl_4$. Examiner also reference Hiroshi as disclosing a process gas that comprises a Si-containing gas where the Si-containing gas comprises at least one of SiH_4, Si_2H_6, or SiH_2Cl_2. (OFFICE ACTION at the bottom of page 11 to page 12.) However, the arguments presented above for claim 1 apply equally to this rejection. Applicants submit that Hiroshi fails to cure the deficiencies of Paton in view of Westlinder and Hareland described above. (RESPONSE TO FINAL REJECTION at page 15, ¶2.)

Regarding claims 10 and 11, Examiner references Christiansen as disclosing the SiGe surface layer comprising a plurality of SiGe sublayers each with different Ge content. Examiner alleges that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Paton accordingly to reduce defects normally present in a single SiGe layer. (OFFICE ACTION at the bottom of page 12 to page 13.) Applicants submit that

Christiansen fails to cure the deficiencies of Paton in view of Hareland and Westlinder set forth above. (RESPONSE TO FINAL REJECTION at page 16, ¶2.)

Regarding claim 17, Examiner further references Edwards as teaching introducing a substrate into a process chamber of a batch-type processing system. (OFFICE ACTION at page 13, ¶3.) Applicants submit that Edwards fails to cure the deficiencies of Paton in view of Hareland and Westlinder as set forth above. (RESPONSE TO FINAL REJECTION at page 16, ¶4.)

In view of the omission of at least one essential element required to establish a *prima facie* rejection of any of the claims, Applicants respectfully assert that the rejections are in error, and Applicants should not be forced through the time and expense of a full-blown appeal.

Respectfully submitted,
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